

A unified modeling and control of a multi-functional current source-typed converter for V2G application

Yao Sun, Weixia Liu, Mei Su, Xing Li, Hui Wang, Jian Yang*

School of Information Science and Engineering, Central South University, Changsha 410083, China

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ABSTRACT

In this paper, a topology based on current source-typed converter (CSC) is proposed for vehicle to grid (V2G) application, which consists of a current-source-type rectifier (CSR) and an auxiliary switching network (ASN). With the help of ASN, this topology is evolved into five circuit structures, and then could be operated in the corresponding five modes: buck charging, boost charging, buck discharging, boost discharging, and reactive power compensation. Therefore, it not only can adapt to a wider range of the battery voltage, but also can provide voltage support to the grid if necessary. For the ease of analysis, a unified mathematical model is established to describe the five operating modes, and a unified control scheme based on active disturbance rejection control (ADRC) idea is proposed to manage the related charging and discharging processes. Experimental results verify the correctness and effectiveness of the proposed topology and control scheme.

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1. Introduction

Due to the increasingly serious energy crisis and global warming issues, the relevant authorities have realized the importance of energy conservation and emission reduction. Developing the plug-in hybrid electric vehicles (EV) or electric vehicles is one of the viable solutions to the above issues [1,2]. In electric vehicle industry, vehicle to grid (V2G) will become an indispensable part in the near future [3,4]. A V2G-capable vehicle could offer reactive power support, active power regulation, load balancing, current harmonic filtering and other services, and then, the efficiency, stability, and reliability of the grid will be enhanced by V2G application [5].

In a V2G system, the bidirectional battery charger plays a critical role, because the charging time and lifecycle of the battery are linked to it [6,7]. Usually, a battery charger of high power density, low volume and cost is expected. Most of the conventional battery chargers are unidirectional, and some of them would cause a large amount of current harmonics in the power grid, which cannot meet the requirements needed by V2G application [6–9]. With the development of power electronics technology, many modern battery chargers contain power factor correction (PFC) circuit and dc/dc converter, where the PFC is used to eliminate harmonic current, and the dc/dc converter adapts the rectified voltage to a level of voltage compatible with the battery voltage. One type of battery charger commonly applied for EV is composed of a voltage

source-type rectifier (VSR) and a dc/dc converter [6,10], formed as a two-stage topology. This type of charger allows bidirectional energy flow, and the input current quality can be improved greatly by the pulse width modulation (PWM) technique. However, the two-stage structure in most occasions may cause high weight and cost, but low efficiency. In addition, the costly, bulky dc-bus capacitor will also affect the lifespan of the charger. According to the duality between the voltage source-typed and current source-typed rectifier (CSR), the CSR would also be suitable for use as a battery charger. Compared to the VSR, the CSR not only offers a compact structure without the costly and bulky electrolytic capacitors, but also can avoid the shoot-through problem by electromagnetic interference (EMI) induced misgating-on [11].

Nowadays, the CSR has been intensively studied as a DC power supply (buck-type rectifier) [12–16]. But in most cases, the energy flow cannot be reversed to the grid. AC/DC matrix converter is one type of CSR with bidirectional switches, which not only allows bidirectional energy flow but also single-stage power conversion. Therefore, it is well suited to V2G application, except for too many semiconductor switches. For the sake of cost reduction, a new topology with fewer controllable switches but more diodes is presented in [17], which is equivalent to AC/DC matrix converter in function. Moreover, an inverting link matrix converter that requires much less switches is presented in [18].

In the research field of battery charger, the configuration of the classic CSR was reported early in [19]. Recently, an AC/DC matrix converter topology with only three switches has been presented applied as a battery charger, and a fuzzy controller is used to overcome the drawbacks caused by the complicated electrochemical

* Corresponding author. Tel.: +86 731 88876070; fax: +86 731 88876070.
E-mail addresses: yaosuncsu@gmail.com (Y. Sun), fish2bear@gmail.com (J. Yang).

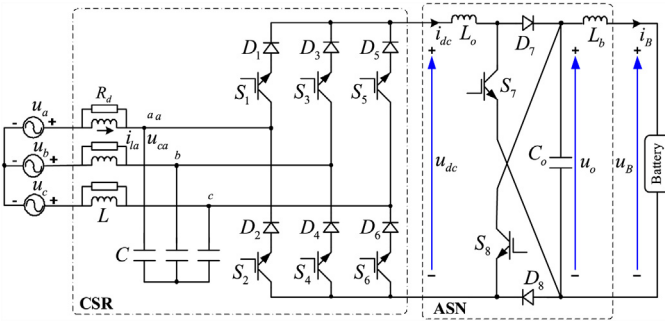


Fig. 1. Proposed topology for V2G application.

battery characteristic [20]. However in the above two cases, the energy stored in the battery cannot be returned to the power grid. Thus, literature [21] proposes one charger topology based on CSR, which allows bidirectional energy flow by using an H-bridge inverter. This topology can be used in V2G application, but the undesired redundant switches may restrict its scope of application. In addition, one type of charger composed of an AC/DC matrix converter and a z-source network is presented in [22], where the charging and discharging is realized by the reconstruction of charger topology. However, it needs a large number of switches, and the related control is relatively complicated.

In this paper, a bidirectional topology based on current source-type converter (CSC) is presented for V2G application, which consists of a classic CSR and an auxiliary switching network (ASN). In this topology, the ASN plays an important role, and helps to complete commutation, voltage boost or buck functions. According to the switching states of the ASN, the proposed converter can be operated in the following five operation modes: buck charging, boost discharging, boost charging, buck discharging and reactive power compensation, which will be analyzed and discussed in detail in the following sections as well as the corresponding control schemes.

The remainder of this paper is organized as follows: Section 2 introduces the topology and mathematic model of the proposed converter. In Section 3, the corresponding control and modulation schemes are presented for the proposed converter. In Section 4, the experimental results are presented, and finally, the main points of this paper are summarized in Section 5.

2. Topology and modeling

2.1. Description of the proposed topology

The proposed CSC topology for V2G application is shown in Fig. 1, which consists of a second-order (LC) input filter, a classic CSR switching circuit, and an ASN. In this topology, the input filter is used to prevent the high-frequency harmonic currents from propagating into the power grid. Note that the damping resistor (R_d) is placed in parallel with the filtering inductor L . The CSR switching circuit contains six insulated gate bipolar transistors (IGBTs) (S_1 – S_6) and six diodes (D_1 – D_6), and each IGBT is connected with a diode in series to obtain the reverse voltage blocking capability. Additionally, the ASN consists of two IGBTs (S_7 – S_8), two diodes (D_7 – D_8), two inductors (L_o , L_b) and a capacitor (C_o).

According to the switching states of S_7 and S_8 , the proposed converter could operate in five modes: Modes I–V. Mode I, i.e. buck charging mode, both the switches S_7 and S_8 are in the off states, and the battery is charged by the rectifier directly. Mode II, i.e. boost discharging mode, S_7 and S_8 are in the on states, and the battery is discharged directly. Mode III, i.e. boost charging mode, S_8 is in the off state, and S_7 is controlled in the PWM way, which means the ASN is functioned as a boost dc–dc converter. Mode IV, i.e. buck

discharging mode, S_7 is in the on state, and S_8 is controlled in the PWM way. Mode V, i.e. reactive power compensation mode, S_7 is in the on state, and S_8 is in the off state, and the system is divided into two independent parts: the static synchronous compensator (STATCOM) and the battery package.

2.2. Operating modes of the proposed topology

For the proposed topology, this subsection will focus on the detailed circuit analysis for different operating modes, in terms of switch states and circuit configurations. First, Fig. 2(a)–(e) shows the corresponding equivalent circuits, when the proposed converter operates in Modes I–V, respectively. Note that in each figure, both the “always on” and “always off” semiconductor devices are omitted, and replaced by the connected and disconnected wires, respectively. The rest are those switches that need to be controlled on and off continually in the operating process.

2.2.1. Mode I (Buck charging mode)

In this mode, both S_7 and S_8 are always in the off states, and the diodes D_7 and D_8 are forward biased. These switches are all omitted in Fig. 2(a), and the inductors L_o and L_b , capacitor C_o constitute a third-order LCL filter. Therefore, the battery is charged from the grid through the classic CSR and LCL filter, which forms a single-stage charging device. The desired charging voltage and current are regulated by the CSR. Due to the structure characteristic, the required charging voltage of battery is no greater than the grid voltage.

2.2.2. Mode II (Boost discharging mode)

Contrary to Mode I, Mode II is about the discharging process with the same single-stage topology, as shown in Fig. 2(b). Due to the unidirectional current of the CSR, both S_7 and S_8 should always be in the on states to complete this discharging mode, and the diodes D_7 and D_8 are blocked naturally. Thus, the energy stored in the battery can be returned to the power grid through the CSR, by controlling the discharging current.

2.2.3. Mode III (Boost charging mode)

In this mode, S_8 is always in the off state, and D_8 is always forward biased; S_7 is set to be switched on or off in the PWM way, and D_7 will bear a forward blocking or forward voltage drop accordingly. Therefore, the ASN works as a boost dc–dc converter as shown in Fig. 2(c), which forms a two-stage charging device combined with the CSR. When S_7 is switched on, the inductor L_o will absorb energy from the grid and the stored energy in the capacitor C_o will be released to the battery. When S_7 is switched off, the capacitor C_o and battery start to absorb energy from the inductor L_o and power grid. Such a mode is needed only when the required charging voltage is greater than the maximum-available rectified voltage.

2.2.4. Mode IV (Buck discharging mode)

As shown in Fig. 2(d), the ASN can be considered a buck dc–dc converter seen from the battery side. In this mode, S_7 is always in the on state, and D_7 is always reverse blocked; S_8 is set to be controlled on or off in the PWM way, and D_8 is reverse blocked or functioned as a freewheeling diode accordingly. When S_8 is switched on, the energy stored in the battery will be transferred to the power grid and L_o . When S_8 is switched off, the inductor L_o will release energy to power grid via the freewheeling diode D_8 . Besides, such a mode can only be operated with the battery voltage being greater than the maximum-available rectified voltage.

2.2.5. Mode V (Reactive power compensation mode)

Unlike the four modes mentioned above, Mode V stresses the reactive power compensation function that the proposed topology can provide, if necessary. In this mode, S_7 is always in the on state,

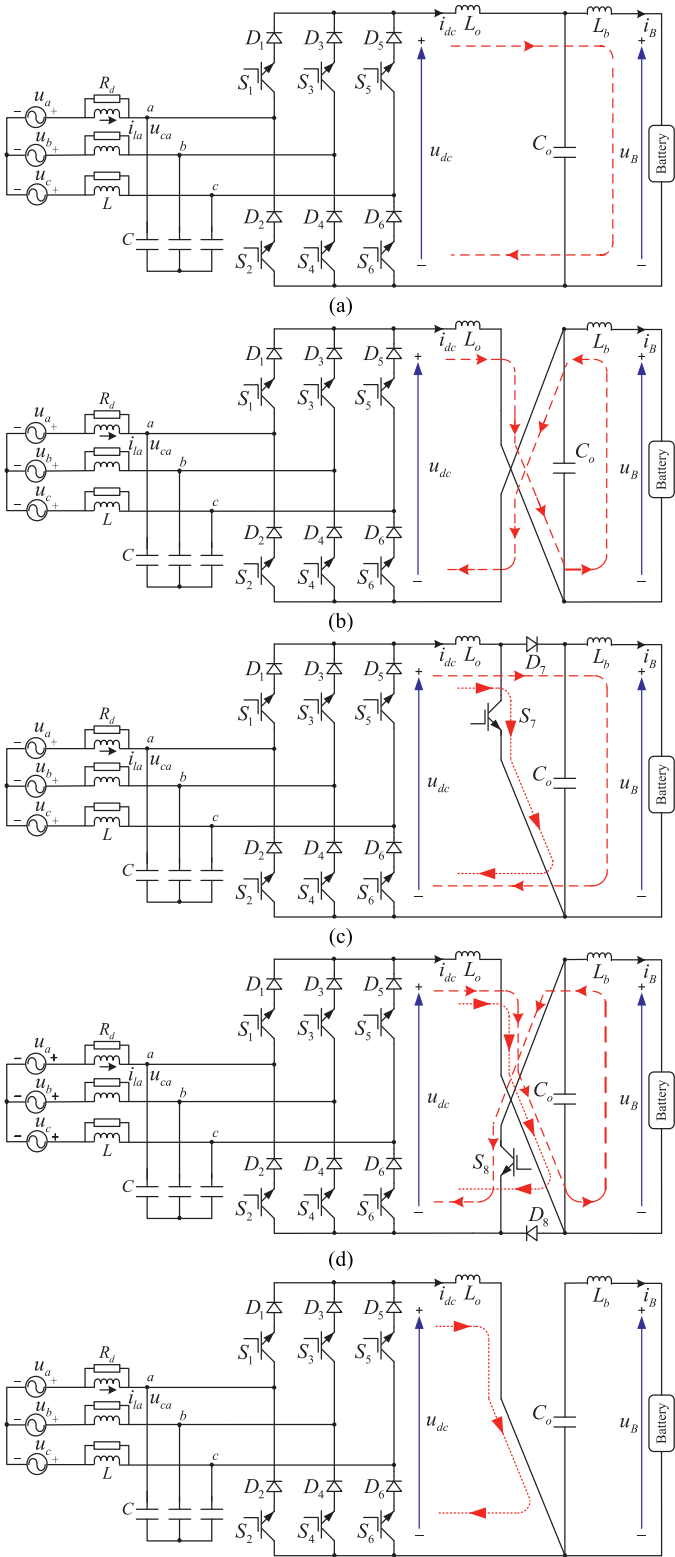


Fig. 2. Equivalent circuits under different operating modes: (a) Mode I, (b) Mode II, (c) Mode III, (d) Mode IV, (e) Mode V.

and D_7 is always blocked; S_8 is always in the off state, and D_8 is always conducted. In that case, the system is divided into two independent parts: a current source-type STATCOM and an isolated battery system, as shown in Fig. 2(e). The STATCOM, composed of the CSR and L_o as the dc-link inductor, can be used to inject reactive current and support the grid voltage, under certain grid faults.

2.3. Average modeling of the proposed topology

Assume that the current through the inductor L_o in all the operating modes is continuous, then, the average modeling method can be applied to obtain the mathematic model of the proposed topology.

First, the dynamics of input filter (ac-part) can be written in space vector representation as:

$$L \frac{d\vec{i}_l}{dt} = \vec{u} - \vec{u}_c \quad (1)$$

$$C \frac{d\vec{u}_c}{dt} = \frac{\vec{u} - \vec{u}_c}{R_d} + \vec{i}_l - i_{dc} \vec{m} \quad (2)$$

where $\vec{u}$ is the grid voltage vector, $\vec{u}_c$ is the voltage vector across the input filter capacitor C , $\vec{i}_l$ and i_{dc} represent the current vectors through the inductors L and L_o , respectively. $\vec{m}$ is the modulation vector of the CSR, and $|\vec{m}| \leq 1$.

According to Fig. 2, the unified dynamic equations for the dc-part can be given as follows:

$$L_o \frac{di_{dc}}{dt} = u_{dc} - \alpha u_o \quad (3)$$

$$C_o \frac{du_o}{dt} = \alpha i_{dc} - i_B \quad (4)$$

$$L_b \frac{di_B}{dt} = u_o - u_B \quad (5)$$

$$u_{dc} = 1.5 (\vec{u}_c \cdot \vec{m}) \quad (6)$$

where u_{dc} is the rectified voltage of CSR, u_o is the voltage across the capacitor C_o , i_B is the charging (or discharging) current, and u_B is the terminal voltage of battery. α represents the circuit parameter that take different values according to different circuit structures. That is: α equals to 1, -1 and 0 in Modes I, II, and V, but $\alpha = 1 - d_7$, $-d_8$ in Modes III and IV, where d_7 and d_8 represent the duty cycles of S_7 and S_8 , respectively. The operator “ $\cdot$ ” in (6) denotes the dot product.

3. Control and modulation scheme

3.1. Control scheme of the proposed topology

In the battery charging, constant current (CC) and constant voltage (CV) modes are widely used, because they consume the shortest time to charge battery fully [23]. First, CC mode is used in the charging process, and the battery terminal voltage should be monitored to avoid overcharging. Once the maximum terminal voltage is reached, CC mode will be replaced by CV mode immediately. Therefore, both CC and CV modes should be considered in the control design of the proposed charging modes. However in the discharging process, the battery is functioned as an independent dc power supply. Thus, to manage the power delivered to the grid, the desired discharging current i_B^* is seen as the control target in the proposed discharging modes.

Usually, the charging process of battery is considered as a complex, uncertain and nonlinear system, and it is not easy to obtain its accurate model. To achieve satisfactory charging performance, a robust control based on ADRC idea is proposed in this section. For the purposes of reliability improvement and cost reduction, only the grid voltages, battery terminal voltage, charging current and the current through inductor L_o are measured.

First, for the single-stage topology in Modes I and II, when CC mode is adopted in the buck charging topology (Mode I), the design procedures of the current control are described as follows.

Denote the reference charging current i_B^* , and the current tracking error is $e_1 = i_B^* - i_B$, according to (3)–(5), the error dynamic equations are given by

$$\begin{aligned} \dot{e}_1 &= e_2 \\ \dot{e}_2 &= e_3 \\ \dot{e}_3 &= bu_{dc} + f\left(u_B, u_o, \frac{d^2 u_B}{dt^2}\right) \end{aligned} \quad (7)$$

where b is the high frequency gain and $b = \frac{-\alpha}{L_b L_o C_o}$, $f(u_B, u_o, \frac{d^2 u_B}{dt^2})$ denotes the unknown disturbance that could be assumed to be bounded, and $f(u_B, u_o, \frac{d^2 u_B}{dt^2}) = \frac{u_o}{L_b C_o} \left(\frac{1}{L_b} + \frac{\alpha^2}{L_o} \right) - \frac{u_B}{L_b^2 C_o} + \frac{1}{L_b} \frac{d^2 u_B}{dt^2} + \frac{d^3 i_B^*}{dt^3}$. For simplicity, the third equation in (7) can be rewritten as

$$\dot{e}_3 = 1.5b(\bar{u} \cdot \bar{m}) + \eta \quad (8)$$

where $\eta = f(u_B, u_o, \frac{d^2 u_B}{dt^2}) + 1.5b(\bar{u}_c \cdot \bar{m} - \bar{u} \cdot \bar{m})$, which can be viewed as the total disturbance of the system. As seen, $\bar{m}$ is the control input, as $\bar{u}$ has been obtained through measurement.

According to the ADRC idea [24,25], an extended state observer (ESO) can be used to estimate the disturbance η in real time, suppose that the estimated disturbance can converge to η precisely and rapidly. To this end, η is viewed as an extended state variable, and will be actively compensated. Using z_1, z_2, z_3 and z_4 to estimate e_1, e_2, e_3 and η , respectively, the ESO can be designed as

$$\begin{cases} \dot{z}_1 = z_2 - \beta_1(z_1 - e_1) \\ \dot{z}_2 = z_3 - \beta_2(z_1 - e_1) \\ \dot{z}_3 = z_4 - \beta_3(z_1 - e_1) + 1.5b(\bar{u} \cdot \bar{m}) \\ \dot{z}_4 = -\beta_4(z_1 - e_1) \end{cases} \quad (9)$$

where $\beta_1, \beta_2, \beta_3$ and β_4 are the observer gains. For simplicity, we can place all the poles of the ESO to the same location or equivalently, and the observer characteristic equation can be formulated as

$$\lambda(s) = \lambda^4 + \beta_1 \lambda^3 + \beta_2 \lambda^2 + \beta_3 \lambda + \beta_4 = (\lambda - \omega_o)^4 \quad (10)$$

where ω_o represents the desired pole location. From (10), once ω_o is well set, $\beta_1, \beta_2, \beta_3$ and β_4 can be solved accordingly.

With the estimated z_1, z_2, z_3 and z_4 , if $\bar{m}$ and $\bar{u}$ are parallel, $|\bar{m}|$ can be constructed as follows:

$$|\bar{m}| = \frac{2}{3|\bar{u}|b}(k_1 z_1 + k_2 z_2 + k_3 z_3 - z_4) \quad (11)$$

where k_1, k_2 and k_3 are the control gains. Substitute (11) into (7) and (8), the error equations become

$$\begin{aligned} \dot{e}_1 &= e_2 \\ \dot{e}_2 &= e_3 \\ \dot{e}_3 &= k_1 e_1 + k_2 e_2 + k_3 e_3 + \zeta \end{aligned} \quad (12)$$

where $\zeta = \eta - z_4 + k_1 e_1 + k_2 e_2 + k_3 e_3$, and $\varepsilon_1 = z_1 - e_1$, $\varepsilon_2 = z_2 - e_2$, $\varepsilon_3 = z_3 - e_3$. Then, if the states and disturbance can be tracked rapidly by the extended observer (9), ζ would be small enough. Therefore, considering the system stability, k_1, k_2 and k_3 should be selected to make the following matrix A being a Hurwitz matrix

$$A = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ k_1 & k_2 & k_3 \end{bmatrix} \quad (13)$$

so, by the appropriate adjustment of the parameters, the current control will be completed with small current tracking error, as

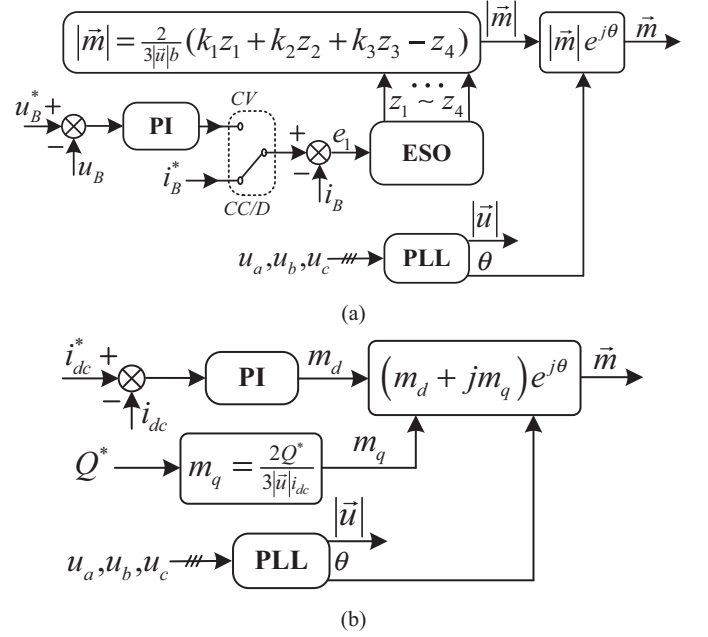


Fig. 3. Block diagrams of the control scheme: (a) Modes I–IV, (b) Mode V.

shown in Fig. 3(a). The stability analysis has been investigated in [23], which is not discussed here in detail.

If the charger operates at CV mode, for simplicity, a dual-loop control structure is adopted as shown in Fig. 3(a), where the outer loop is voltage control using a proportional-integral (PI) controller, and the inner loop is the current control mentioned above. As seen, “CC”, “CV” and “D” represents the CC and CV charging modes, and discharging mode, respectively, and the single-pole, two-throw switch is used to select these modes.

As for the two-stage topology in Modes III and IV, there are two degrees of freedom ($|\bar{m}|$ and α) that can be used to complete the control design of the system: $|\bar{m}|$ is for the CSR and α is for the dc-dc converter formed by the ASN. For the sake of simplicity, one of them can be predetermined as required, and the other is mainly responsible for the regulation of the charging current or voltage. If $|\bar{m}|$ is assigned to a fixed value, then α should be used to control the charging/discharging process. However, it has to be noted that such a system is a non-minimum phase system, where the unstable zero will degrade the control performance. To overcome this drawback, α is assigned to a fixed value in accordance with the actual voltage step up/down situation, and $|\bar{m}|$ is in charge of controlling the charging current or voltage here. Moreover, there is another advantage for the above arrangement, which is the control configuration used in Modes I and II can be retained for Modes III and IV.

In Mode V, the converter has been reduced to the current source-typed STATCOM and the isolated battery, which are independent of each other. Thus, the control design of the STATCOM does not rely on the charging or discharging current, whose purpose is the reactive power transmitted to the grid. Since the input currents are not measured, a simple open-loop control for reactive power is proposed here, as shown in Fig. 3(b). As seen, the d -axis component m_d of $\bar{m}$ (in grid voltage orientation) is obtained by regulating the current i_{dc} properly using a PI controller, which is used to compensate the converter power loss. Usually, the current through the input filter capacitor and m_d are relatively small, then, the desired reactive power Q^* generated by the STATCOM (originally $1.5|\bar{u}|i_q$, where i_q is the reactive component of the input current) can be

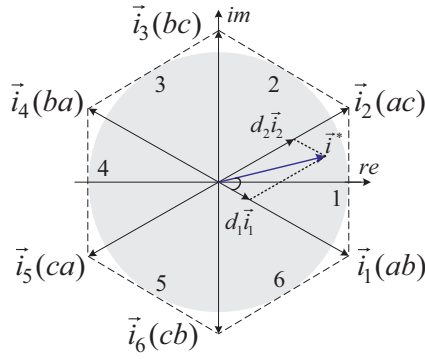


Fig. 4. Schematic diagram for the classic current space vector modulation.

approximated as $1.5 |\vec{u}| i_{dc}^* m_q$. Thus, the q -axis component m_q can be obtained consequently.

3.2. Modulation method of the proposed topology

3.2.1. Modulation for the CSR

The classical current space vector modulation (SVM) strategy is introduced here for the CSR briefly, which is used in all the operating modes of the proposed topology. According to the desired input current vector $\vec{i}^*$, six active vectors $\vec{i}_1$ – $\vec{i}_6$ and three zero vectors $\vec{i}_7$ – $\vec{i}_9$ are used to synthesize it, where each vector corresponds to a switching state of the rectifier, as shown in Fig. 4. The principles of the sector division in this modulation strategy are as follows: sector 1 is between $\vec{i}_1$ and $\vec{i}_2$; sector 2 is between $\vec{i}_2$ and $\vec{i}_3$, and so forth. In any sector, two adjacent active vectors and a zero vector are used to synthesize the required input current vector.

In this paper, $\vec{i}^*$ is determined by the control output $\vec{m}$ and the measured i_{dc} . Therefore, without loss of generality, if $\vec{i}^*$ is located in the sector 1, $\vec{i}_1$, $\vec{i}_2$ and $\vec{i}_7$ will be used. Based on the principle of capacitor charge balance, the corresponding duty cycles can be expressed as follows:

$$\begin{cases} d_1 = |\vec{m}| \sin\left(\frac{\pi}{3} - \varphi\right) \\ d_2 = |\vec{m}| \sin(\varphi) \\ d_0 = 1 - d_1 - d_2 \end{cases} \quad (14)$$

where d_1 , d_2 and d_0 are the duty cycles of the vector $\vec{i}_1$, $\vec{i}_2$, and $\vec{i}_7$, respectively. φ is the angle between $\vec{i}^*$ and the vector $\vec{i}_1$ in the sector 1. Similarly, if $\vec{i}^*$ is located in the other sectors, the corresponding duty cycles could also be obtained in the same way as mentioned above.

3.2.2. Modulation for the ASN

In Modes I, II and V, S_7 and S_8 in the ASN are always in the on/off states, which are arranged as: $S_{7/8} = 0$ if the switch is on and $S_{7/8} = 1$ if the switch is off. In mode III and IV, S_7 or S_8 works in the PWM way, and the trigger signals are obtained by comparing the modulated wave m_1 (d_7 or d_8) and the triangle carrier signal. The corresponding schematic diagram of modulation is shown in Fig. 5, including those of the CSR and ASN under Modes I–V. As seen in the figure, “I”–“V” denote the Modes I–V, respectively, and the single-pole three-throw switch is used to select the operating modes. Additionally, to further reduce the charging current ripple, the bilaterally symmetrical switching pattern is adopted here. Taking Mode III as an example, the switching pattern arrangement is illustrated in Fig. 6.

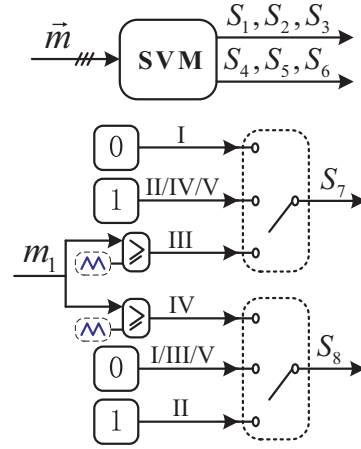


Fig. 5. Modulation diagram of the CSR and ASN in Modes I–V.

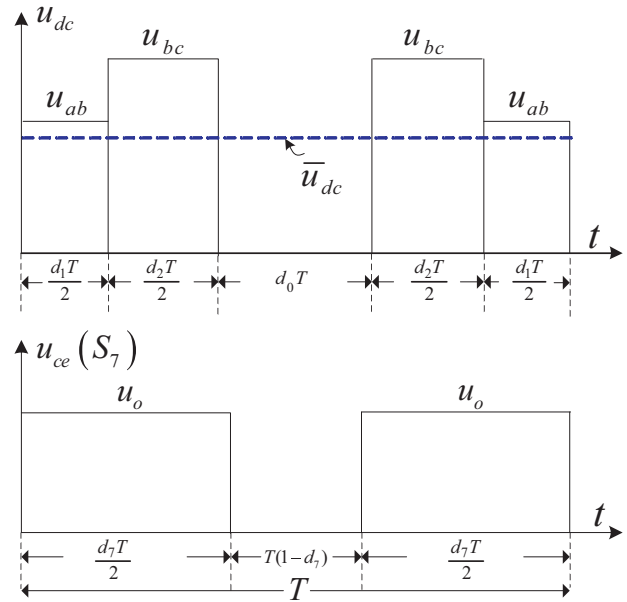


Fig. 6. Switching pattern arrangement for Mode III.

4. Experimental results

To verify the feasibility of the proposed topology and related control scheme, a prototype for this converter has been built in the laboratory, as shown in Fig. 7. The controller board is mainly composed of a digital signal processor (DSP) TMS320F28335 and a field programmable gate array (FPGA) EP2C8T144C8 N. The IGBTs used in the main circuit are 1MBH60D-100, and the fast recovery diodes are DSEI30-12A. The parameters used in the experiments are listed in Table 1.

Table 1
Parameters used for AD/DC matrix converter simulation.

Parameters	Vaule
Input phase voltage	40 V(rms)
Input filter inductor	0.6 mH
Input filter capacitor	20 μ F
Filter inductor L_o	5 mH
Output filter capacitor C_o	20 μ F
Filter inductor L_b	0.4 mH
Switching frequency	10 kHz

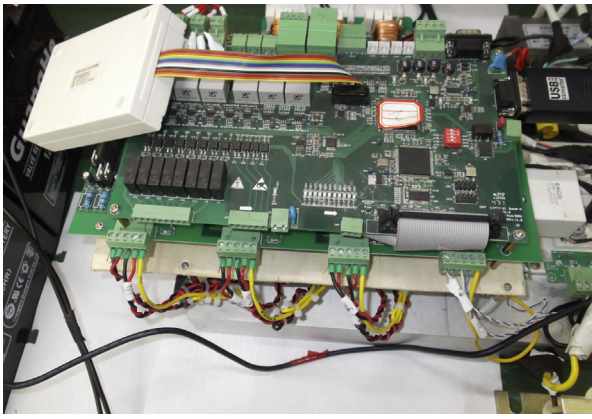


Fig. 7. Prototype of the proposed topology built in the laboratory.

Two groups of lead-acid battery pack are used in the experiment, and the specifications are 60 V/40 Ah and 120 V/40 Ah, respectively. Since the input voltage is set to 40 V (rms), the average maximum output voltage of the CSR that can be obtained is 85 V approximately, which can meet all the requirements of the experiment.

When the lead-acid battery pack of 60 V/40 Ah is connected to the converter operated in Mode I, two cases (CC and CV modes) are tested. In CC mode, the desired charging current i_B^* is set to 4 A, and Fig. 8 shows the experimental waveforms (5 ms/div) of the input voltage u_a , input current i_a , dc-link voltage u_{dc} , and the charging current i_B . As seen, the input current is sinusoidal and in phase with the input voltage; the charging current tracks its reference well with small ripple. In CV mode, the desired charging voltage u_B^* is set to 67.5 V, and Fig. 9 shows the corresponding experimental results (5 ms/div) of the input voltage u_a , input current i_a , battery voltage u_B , and the charging current i_B . From Fig. 9, it can be found that the charging voltage tracks its reference well.

When the converter is operated in Mode II, the energy stored in the battery can be delivered to the power grid. In that case, if the desired discharging current i_B^* is set to 4 A, the corresponding experimental results (5 ms/div) are illustrated in Fig. 10, including the input voltage u_a , input current i_a , dc-link voltage u_{dc} , and the discharging current i_B . As seen, the input current is out of phase with the input voltage, which indicates the battery is providing energy back to the grid. Moreover, the polarity of the output voltage of CSR is opposite to that in Mode I.

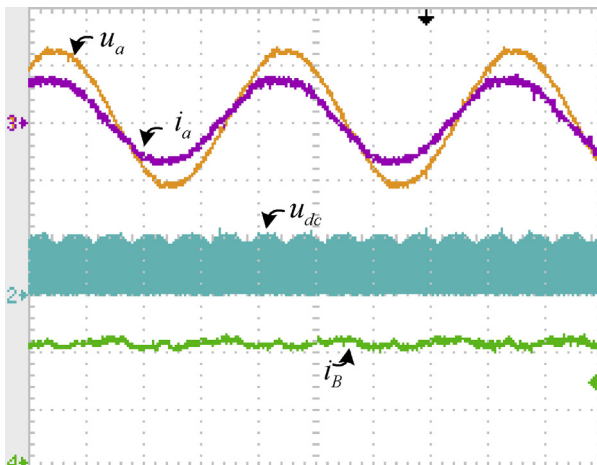


Fig. 8. Waveforms of the input voltage (50 V/div), input current (5 A/div), output voltage of CSR (100 V/div), and charging current (2 A/div) in Mode I at CC mode.

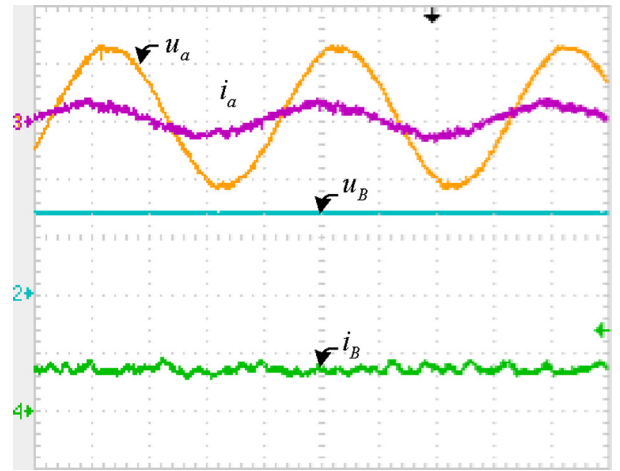


Fig. 9. Waveforms of the input voltage (50 V/div), input current (5 A/div), terminal voltage of battery (50 V/div), and charging current (2 A/div) in Mode I at CV mode.

To test the dynamic response of the proposed converter with regard to disturbance, the desired charging current i_B^* is changed from 2 A to 4 A suddenly in Mode I. The transient response of the input voltage u_a , input current i_a , dc-link voltage u_{dc} , and the charging current i_B with different pole locations and controllers are shown in Fig. 11 (10 ms/div), where Fig. 11(a) shows the experimental results referred to the basic case with the proposed controller based on ADRC and normalized pole location ($\omega_o = 100$). If ω_o get enlarged ($\omega_o = 170$), the corresponding waveforms are shown in Fig. 11(b), it can be found that the charging current tracks its reference faster than that in Fig. 11(a). Moreover, if a PI controller is utilized instead of the controller based on ADRC (without the extended state observer), the related experimental results are shown in Fig. 11(c). As seen, compared to those in Fig. 11(a), the response becomes slow, and a low frequency oscillation appear in the charging current. Therefore, it can be concluded that the proposed control scheme with a proper selection of the observer gains can achieve good control performance. Furthermore, when the converter operation is changed from Mode I ($i_B^* = 2$ A) to Mode II ($i_B^* = -2$ A), the corresponding experimental waveforms are shown in Fig. 12 (10 ms/div).

When the lead-acid battery pack of 120 V/40 Ah is connected to the converter operated in Mode III, the desired charging current i_B^* is set to 4 A at CC mode, while the desired charging voltage u_B^* is set to 135 V at CV mode. Figs. 13 and 14 show the related experimental

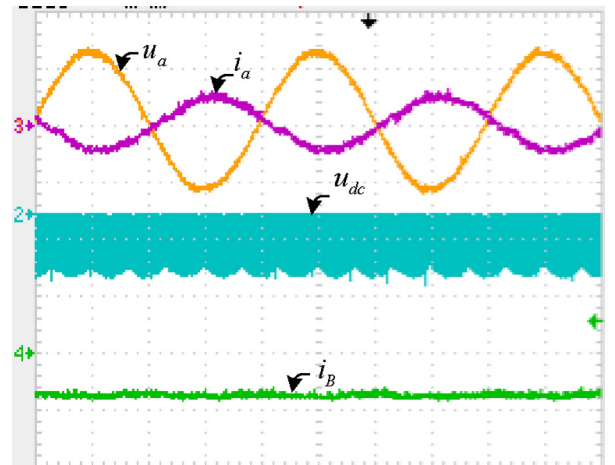


Fig. 10. Waveforms of the input voltage (50 V/div), input current (5 A/div), output voltage of CSR (100 V/div), and discharging current (5 A/div) in Mode II.

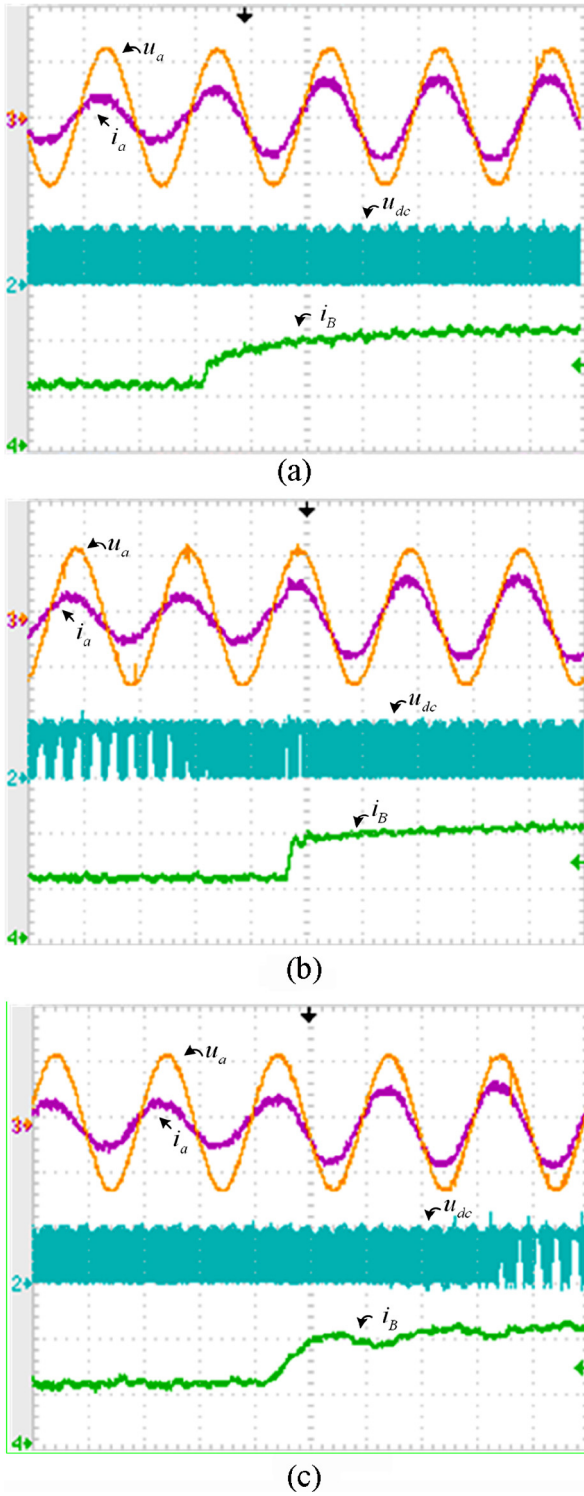


Fig. 11. Waveforms of the input voltage (50 V/div), input current (5 A/div), output voltage of CSR (100 V/div), and charging current (2 A/div) in Mode I at CC mode with the reference charging current variation from 2 A to 4 A: (a) $\omega_0 = 100$; (b) $\omega_0 = 170$; (c) without ADRC.

results (5 ms/div) at CC and CV mode, respectively. When the converter is operated in Mode IV, Fig. 15 shows the experimental results (5 ms/div) with $i_B^* = -4$ A. All the results indicate that the converter could work well in these modes. Note that in the above experiments, $\alpha = 0.5$ in Mode III; $\alpha = -0.5$ in Mode IV.

In Mode V, the current through L_o is controlled to be 7.5 A. Fig. 16(a) and (b) shows the experimental waveforms (5 ms/div) of the input voltage u_a , input current i_a , dc-link voltage u_{dc} , and

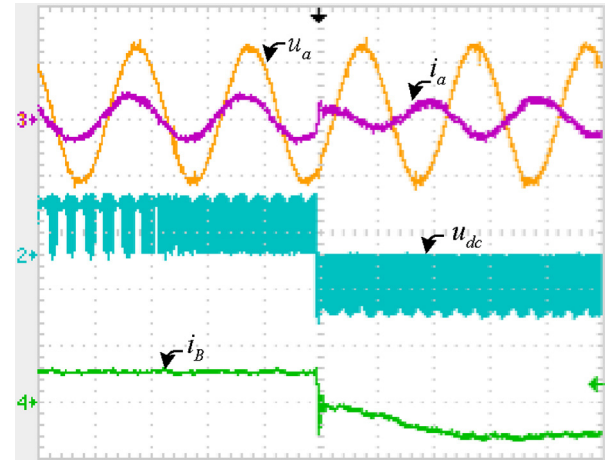


Fig. 12. Waveforms of the input voltage (50 V/div), input current (5 A/div), output voltage of CSR (100 V/div), and charging current (4 A/div) with the variation from Mode I to Mode II.

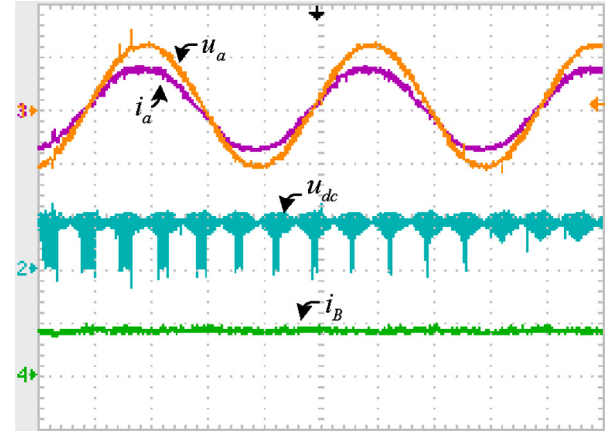


Fig. 13. Waveforms of the input voltage (50 V/div), input current (10 A/div), output voltage of CSR (100 V/div), and charging current (5 A/div) in Mode III at CC mode.

the current through the inductor (L_o) i_{dc} , when the desired reactive power Q^* is set to 425VAR, and -425 VAR, respectively. As seen, from Fig. 16(a), the input voltage is before the input current of a phase angle of 90° , and in Fig. 16(b), the input voltage are behind the input current of 90° approximately.

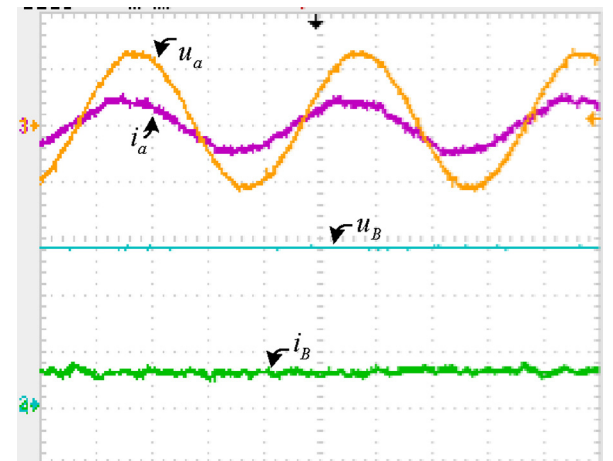


Fig. 14. Waveforms of the input voltage (50 V/div), input current (5 A/div), terminal voltage of battery (50 V/div), and charging current (2 A/div) in Mode III at CV mode.

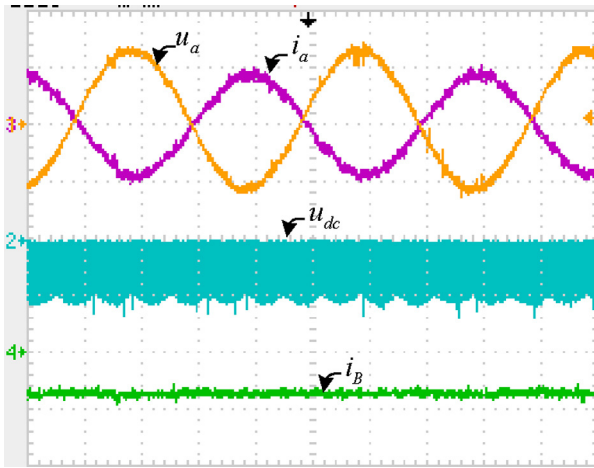


Fig. 15. Waveforms of the input voltage (50 V/div), input current (5 A/div), output voltage of CSR (100 V/div), and discharging current (5 A/div) in Mode IV.

In addition, the converter efficiency in the buck charging, boost charging, boost discharging and buck discharging modes are measured by a power analyzer, and the corresponding efficiency curves are shown in Fig. 17. As seen, the efficiency in the charging modes is higher than those in the discharging modes. In the charging modes,

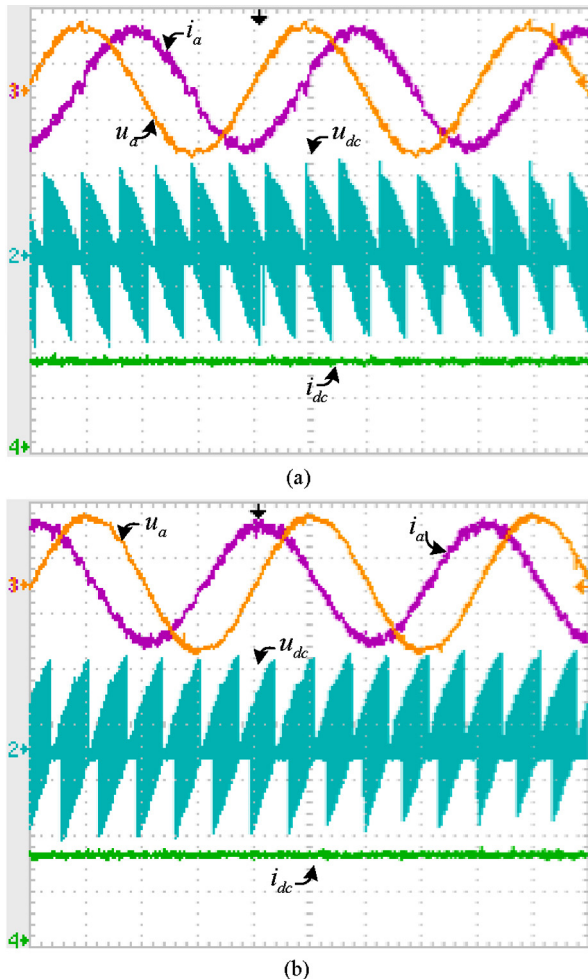


Fig. 16. Waveforms of the input voltage (50 V/div), input current (5 A/div), output voltage of CSR (100 V/div), and current through inductor L_o (5 A/div) in Mode V: (a) $Q^* = 425\text{VAR}$, (b) $Q^* = -425\text{VAR}$.

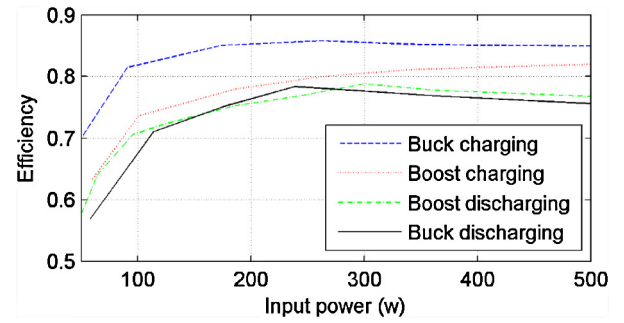


Fig. 17. Efficiency curves in the buck charging, boost charging, boost discharging and buck discharging modes.

the efficiency in the buck mode is higher than that in the boost mode; while in the discharging mode, the differences between the modes are not too obvious. Additionally, the efficiency in all the modes are not very high, there are several reasons for it. First, the input voltages used in the experiment are relatively low, which makes the conduction loss large. Second, the prototype in the lab is not designed for optimal efficiency, and it is built mainly to verify the correctness and effectiveness of the proposed topology and control scheme. At last, to realize the multiple functions, some extra switches are needed, and it is difficult to avoid the associated power losses.

5. Conclusions

In this paper, a bidirectional CSC topology is proposed as a grid interface for V2G application, which can be used to perform multiple functions, including the charging and discharging of battery, and reactive power compensation. In essence, it is a dual of the converter composed of a voltage source-typed rectifier and a bidirectional buck converter. By contrast, it is more suitable for the application where the desired charging voltage is less than the maximum-available rectified voltage due to the advantage of high efficiency. All the operation modes of the proposed topology are analyzed in detail, and a unified mathematical model is established for the dynamics in different modes. To achieve satisfactory charging performance with fewer sensors, a robust control based on ADRC idea is presented. It is verified by experiments that, the proposed topology and the related control method are correct and effective, which may become a promising candidate in A2G application.

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